REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-10 are presently pending in the present application. Claims 1-6 have been amended and claims 7-10 have been added by way of the present Amendment. No new matter is introduced by this amendment.

Applicants note that the Office Action cites *Meyers et al.* (U.S. Patent No. 6,771,096) in the obviousness rejection of claim 4; however, this reference was not listed on Form PTO-892 attached to the Office Action. Accordingly, Applicants respectfully request that *Meyers et al.* be officially placed on the record by listing this reference on a Form PTO-892 attached to the next Office communication from the Patent Office.

In the Office Action, claim 2 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite; claims 1-3, 5, and 6 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Asami* (U.S. Patent No. 4,904,948); and claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Asami* in view of *Meyers et al.* (U.S. Patent No. 6,771,096).

Regarding the indefiniteness rejection of claim 2, claim 2 has been amended to remove the phrase "whose frequency may be divided if required." Accordingly, Applicants respectfully request the withdrawal of the indefiniteness rejection.

Regarding the rejection of claims 1-6 under 35 U.S.C. §103(a), Applicants respectfully request the withdrawal of the obviousness rejection for the reasons set forth below.

The basic requirements for establishing a *prima facie* case of obviousness as set forth in MPEP §2143 include (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, (2) there must be a reasonable expectation of

success, and (3) the reference (or references when combined) must teach or suggest all of the claim limitations. Applicants submit that a *prima facie* case of obviousness cannot be established in the present case because the cited reference does not teach or suggest all of the claim limitations.

Independent claims 1 and 6 each recite, among other features, a phase/frequency comparator having two edge-triggered storage devices that "are each reset by a resetting signal that is output from a resetting logic unit," "said resetting logic unit having inputs that are supplied with the output signals from the two edge-triggered storage devices, wherein the resetting signal from the resetting logic unit is only activated when both the output signals from the two edge-triggered storage devices have been activated, and is only de-activated when both the output signals from the two edge-triggered storage devices have been deactivated, wherein the resetting logic unit includes an asynchronous level-triggered RS storage device of inverse logic, the resetting input of the asynchronous level-triggered RS storage device having an output signal from an OR gate supplied to it, and **wherein the two edge-triggered storage devices each have only a single output, the single output of each of the two edge-triggered storage devices being of non-inverted logic**."

At the outset, the Applicant submits that recent Supreme Court and Federal Circuit decisions have not removed the burden on the Patent Office of establishing a *prima facie* case of obviousness by providing evidentiary support for the conclusion that the features recited in the claims, as well as any asserted rationale for combining or modifying such features to arrive at the claimed invention, were known at the time of the present invention. Many of these cases in fact dealt with situations where all of the limitations were taught in various cited references, and the issue was whether there was a reason at the time of the invention to combine the teachings in those references to arrive at the claimed invention. To the contrary, in the present situation, the

issue at hand is the failure to establish a *prima facie* case of obviousness, since there is no evidentiary support for the conclusion that the features recited in the claims and the asserted rationale for combining or modifying such features to arrive at the claimed invention were known at the time of the present invention.

MPEP §2141 notes that the Patent Office bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. MPEP §2141 emphasizes that "Office personnel fulfill the critical role of factfinder when resolving the *Graham* inquiries. .... When making an obviousness rejection, Office personnel must therefore ensure that the written record includes findings of fact concerning the state of the art and the teachings of the references applied. .... Factual findings made by Office personnel are the necessary underpinnings to establish obviousness." MPEP §2142 further notes that "[t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. .... Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the "differences," conduct the search and evaluate the "subject matter as a whole" of the invention. .... However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art."

The Office Action indicates that *Asami* teaches all of the features recited in independent claims 1 and 6 including the recitation of two edge-triggered storage devices each having only an output of non-inverted logic, with the exception of the limitation directed to the OR gate. However, the Office Action asserts that it is notoriously well known in the art that an OR-function can be implemented both by an OR-gate with non-inverted signals and by an NAND-gate with inverted signals and that both circuit arrangements are mutually interchangeable, without any unexpected results in circuit operation. The Office Action then concludes that "it

would have been obvious to one skilled in the art at the time of the applicant's invention was made to replace the NAND- gate (NG3 of Asami) with an OR-gate for the expected advantage of reducing wiring overheads."

At the outset, Applicant submits that the Office Action fails to provide any evidentiary support for the assertion that it was known at the time of the present invention to interchange components in a manner that would arrive at the present invention, as suggested in the obviousness rejection. Additionally, the Office Action fails to provide any evidentiary support for the assertion that it was known at the time of the present invention to make such a modification "for the expected advantage of reducing wiring overheads." Accordingly, the Patent Office has failed to fulfill the critical role of factfinder, and has therefore failed to satisfy the initial burden of factually supporting any *prima facie* conclusion of obviousness. Thus, the Applicant requests that such evidentiary support be placed on the record, or the obviousness rejection withdrawn.

Furthermore, the Office Action asserts that *Asami* teaches two edge-triggered storage devices each having only an output of non-inverted logic. However, the Applicant respectfully disagrees. Claims 1 and 6 have been amended merely for clarification to recite that "the two edge-triggered storage devices each have only a single output, the single output of each of the two edge-triggered storage devices being of non-inverted logic." The Applicant respectfully submits that *Asami* fails to disclose or suggest such features.

Asami describes a phase comparator circuit that includes a first flip-flop circuit (1), a second flip-flop circuit (2), and a latch circuit (3), as shown in Fig. 5. The phase comparator circuit compares a phase of a first input signal (A) with that of a second input signal (B). The first flip-flop circuit (1) receives the first input signal (A) and outputs a first output signal (O_A) and an inverted signal (O_a), and the second flip-flop circuit (2) receives the first input signal (B)

and outputs a second output signal (O_B) and an inverted signal (O_b). Fig. 6 shows an embodiment of such a phase comparator circuit that includes a first D-type flip-flop circuit (1) with a first input signal (A) and a second D-type flip-flop circuit (2) with a second input signal (B). On the output sides, **two** lines are leaving the circuits. On the output side of the first D-type flip-flop circuit (1), the signal (O_A) is output on output terminal (Q_{1A}) and its inverted signal (O_a) is output on output terminal (Q_{1a}). On the output side of the second D-type flip-flop circuit (2), the signal (O_B) is output on output terminal (Q_{1B}) and its inverted signal (O_b) is output on output terminal (Q_{1b}). The two signals (O_A) and (O_B) are connected to a first NAND gate circuit (NG_1) of the latch circuit (3), whereas the two inverted signals (O_a) and (O_b) are connected to a third NAND gate circuit (NG_3). Thus, four lines have to be located between the flip-flops and the latch circuit.

Contrary to the above, claims 1 and 6 recite that "the two edge-triggered storage devices each have only a single output, the single output of each of the two edge-triggered storage devices being of non-inverted logic." By way of illustration and not limitation, Fig. 4 in conjunction with Fig. 3 of the application depicts a non-limiting embodiment of the present invention in which a reference-frequency signal (3) enters a first flip-flop (13), but only one output signal (9A) leaves the flip-flop and enters the resetting logic (15). The output-frequency signal (6) enters a second flip-flop (14) on the input side, and only one signal (9B) leaves the flip-flop and enters the resetting logic (15). At the resetting logic (15), the lines are duplicated and signal (9A) and signal (9B) are input to the first gate (i.e., NAND in Fig. 4) and a second gate (i.e., OR in Fig. 4), respectively.

The two-edge-triggered storage devices defined in claims 1 and 6 each have only a single output. *Asami* fails to disclose or suggest such a feature, since each of the flip-flop circuits (1) and (2) clearly have two outputs, namely, output terminal (Q_{1A}) and output terminal (Q_{1a}) for

circuit (1), and output terminal (Q_{2B}) and output terminal (Q_{2b}) for circuit (2). The present invention advantageously reduces cabling effort as compared to the configuration in *Asami* (i.e., four terminations at flip-flop circuits and four terminations in the latch circuit in *Asami* versus only two terminations at the edge-triggered storage devices and two terminations on the resetting logic of the claims), as well as the subsequent reduction in space consumption. Additionally, with the configuration of the present invention, no effort needs to be taken to generate inverted versions of the output signals of the edge-triggered storage devices. Clearly, *Asami* failed to disclose or suggest the recited features, and failed to contemplate the benefits afforded by the present invention. Thus, the Applicant submits that there is no evidentiary support for the assertion that it would have been obvious at the time of the present invention to use the OR gate with edge-triggered storage devices each having only a single output, the single output of each of the two edge-triggered storage devices being of non-inverted logic. The inventive character of the present invention is even more evident from a review of the second embodiment of the resetting logic of the present invention shown in Fig. 5 of the present application.

Accordingly, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established with respect to independent claims 1 and 6. Thus, the Applicant requests the withdrawal of the obviousness rejection of claims 1 and 6.

The dependent claims are considered allowable for the reasons advanced for independent claim 1 from which they depend. These claims are further considered allowable as they recite other features of the invention that are neither disclosed nor suggested by the applied references when those features are considered within the context of independent claim .

Therefore, the present application, as amended, overcomes the rejections of record and is in condition for allowance. Favorable consideration is respectfully requested. If any unresolved issues remain, it is respectfully requested that the Examiner telephone the

undersigned attorney at (703) 519-9957 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,

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Date

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